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DATE: Wednesday, June 21, 2006

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<input type="checkbox"/>	L33	L32 and (revers\$ with mapping)	1
<input type="checkbox"/>	L32	L31 and ((data adj1 structure) with definition\$ with mapping)	10
<input type="checkbox"/>	L31	707/100-101.ccls.	6295
<input type="checkbox"/>	L30	L29 and (revers\$ or undo\$ or back\$)	1
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<input type="checkbox"/>	L23	L22 and priority	1
<input type="checkbox"/>	L22	20040093342.pn.	2
<input type="checkbox"/>	L21	L20 and (mapping near definition)	1
<input type="checkbox"/>	L20	L19 and mapping.ti.	43
<input type="checkbox"/>	L19	(previous near mapping)	370
<input type="checkbox"/>	L18	(prior with (mapping near definition))	1
<input type="checkbox"/>	L17	(previous with (mapping near definition))	2
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<input type="checkbox"/>	L16	(former with (mapping near definition))	1
<input type="checkbox"/>	L15	(past with (mapping near definition))	0
<input type="checkbox"/>	L14	(before with (mapping near definition))	4
<input type="checkbox"/>	L13	(earl\$ with (mapping near definition))	0
<input type="checkbox"/>	L12	(previous with (mapping near definition))	2
<input type="checkbox"/>	L11	(prior with (mapping near definition))	1
<input type="checkbox"/>	L10	(prior near mapping near definition)	0
<input type="checkbox"/>	L9	(previous near mapping near definition)	0
<input type="checkbox"/>	L8	L6 and (mapping with structures)	5
<input type="checkbox"/>	L7	L6 and (mapping near structures)	0
<input type="checkbox"/>	L6	L5 and mapping.ti.	42
<input type="checkbox"/>	L5	(map\$ near definition)	705

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DB=USPT; PLUR=NO; OP=OR

- ☐ L4 L2 and (conver\$ or map\$ or transform\$).ti. 10
- ☐ L3 L2 and (conver\$ or map\$ or transform\$) 45
- ☐ L2 L1 and (software or application\$ or program\$).ti. 46


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TitleConcurrent **data** structures for hypercube machine.**Conference information**

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Abstract

To efficiently implement parallel algorithms on parallel computers, concurrent **data** structures (**data** structures which are simultaneously updatable) are needed. In this paper, three implementations of a priority queue on a distributed-memory **message** passing multiprocessor with a hypercube topology are presented. In the first implementation, a linear chain of processors is mapped onto the hypercube, and then a heap **data structure** is mapped onto the chain, where each processor stores one level in the heap. A similar approach is taken for the second implementation, but in this case, a banyan heap **data structure** is mapped onto the linear chain of processors. Again, each processor in the chain becomes responsible for one level of the **data structure**. For the third implementation, the banyan heap **data structure** is again used, but the **mapping** is not onto linear chain of processors. Instead, the banyan heap is mapped onto processors column by column, so that the algorithm can make better use of the concurrent processing capabilities of the hypercube topology in order to reduce bottlenecking in the first processor, an effect noted in the use of the linear chain employed by the first two implementations. The key advantage of banyan heap over the heap is that with banyan heap it is possible to retrieve elements at different percentile levels.

Descriptors

 [DATA-STRUCTURES](#);  [DISTRIBUTED-MEMORY-SYSTEMS](#);  [HYPERCUBE-NETWORKS](#);
 [PARALLEL-ALGORITHMS](#).

Classification codes[C4240P](#) [Parallel-programming-and-algorithm-theory*](#);

C5220P Parallel-architecture;
C4230M Multiprocessor-interconnection.

Keywords

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